REMARKS

By this amendment, claims 1 and 15 have been amended. Claims 3, 11-15, and 17 have been withdrawn. New claims 42-43 have been added. Claims 1-5, 8-18, 20-21, and 41-43 are pending in the application. Applicants reserve the right to pursue the original claims and other claims in this and other applications.

Claims 1-2, 4-5, 7-9, 15, 17, 19, 20, and 40-41 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Merrill et al. (US 6,512,544) in view of Sauer (US 6,320,616). This rejection is respectfully traversed. In order to establish a *prima facie* case of obviousness "the prior art reference (or references when combined) must teach or suggest all the claim limitations." M.P.E.P. §2142. Neither Merrill et al. nor Sauer, even when considered in combination, teaches or suggests all limitations of independent claims 1 and 15.

Claim 1 recites a method of processing pixel signals comprising, *inter alia*, "clamping a pixel readout line to a voltage level less than a voltage corresponding to a pixel signal; subsequently ... reading out the pixel signal onto the pixel readout line; subsequently clamping a capacitive storage node in a pixel signal processing circuit to a voltage higher than a voltage corresponding to the pixel signal appearing on the pixel readout line" (emphasis added). Claim 15 recites similar limitations for an imager. Amendments to claims 1 and 15 conform to the original disclosure, where, for example, the capacitive storage node 60 is pre-charged to a predetermined relatively high voltage level. *See* Specification, page 9, ln. 11-34. Applicants respectfully submit that Merrill et al. and Sauer, even when combined, do not teach or suggest these limitations.

To the contrary, Sauer teaches that "the light signal charge stored in photodetector 116 is switched onto FD node 115, causing a negative going signal voltage step on the Col_Read(x) line. ... [T]he voltage at FD node 115 falls ..., and the voltage on the Col_Read(x) line falls from 3.801 V to 2.801 V.... While SH remains high, the new output voltage on the Col_Read(x) line (2.801 V) is applied across capacitor C1 at node 157 ... [which] is indicative of the amount of light sensed." Col. 8, ln. 13-24 (emphasis added). Therefore, the same voltage is applied at node 157 as that applied to the column line, which corresponds to the pixel signal. Applicants respectfully submit that Sauer does not disclose, teach, or suggest reading out the pixel signal and subsequently clamping a capacitive storage node to a voltage higher than a voltage corresponding to the pixel signal appearing on the pixel readout line, as recited in claims 1 and 15. Nor does Merrill et al. teach or suggest these limitations. Thus, Merrill et al. does not remedy the deficiencies of Sauer.

Moreover, even if Sauer were to disclose reading out the pixel signal and subsequently clamping a capacitive storage node to a voltage higher than a voltage corresponding to the pixel signal, which it does not, Applicants respectfully submit that Merrill et al. and Sauer are not properly combinable. Indeed, the combination of the Merrill et al. and Sauer would contradict the teachings of Merrill et al. and render the Merrill et al. device inoperable. In order to function, Merrill et al. requires that the column line 108 be reset to a ground potential before pixel readout. (Col. 6, ln. 51-52, FIG. 7).

Conversely, in order to function, Sauer requires that the column line Col_Read(x) must be clamped to 3.801 V before pixel readout. Sauer teaches that "the output voltage on the Col_Read(x) line is approximately 3.8 V+kTC noise=3.801 V, in the period before the photo signal charge is transferred to FD node 115. The voltage (3.801 V) on the

Col_Read(x) line at this stage may be referred to as the APS reference voltage." Col. 7, ln. 14-18 (emphasis added). Sauer further teaches that while the clamp pulse CL and sample-and-hold pulse SH are high, "the APS reference voltage of 3.801 V [is] applied to node 157." Col. 7, ln. 35-39. In order to function, Sauer requires that both the column line Col_Read(x) and the node 157 be clamped to a high voltage (i.e., 3.801 V) before the pixel signal is read out.

Combining Sauer's requirement of clamping the column line to 3.801 V with Merrill et al.'s requirement of clamping the column line to ground would contradict and render inoperable the teachings of Merrill et al., and vice versa. Accordingly, the references are inherently not combinable, as using the teachings of one reference in combination with the other would destroy the teachings of the other.

Since Merrill et al. and Sauer do not teach or suggest all of the limitations of claims 1 and 15, nor are they combinable, claims 1 and 15 are not obvious over the cited references. Claims 2, 4-5, 7-9, 17, 19, 20, and 40-41 depend, respectively, from independent claims 1 and 15, and are patentable at least for the reasons mentioned above, and on their own merits. Applicants respectfully request that the 35 U.S.C. § 103(a) rejection of claims 1-2, 4-5, 7-9, 15, 17, 19, 20, and 40-41 be withdrawn and the claims allowed.

In addition, new claims 42-43 recite that "the capacitive storage node comprising a binary scaled capacitor network." Sauer teaches in FIG. 1 only the individual capacitors C1, C2, and C5, but is silent with respect to any values or respective values for the capacitors. Applicants respectfully submit that Sauer does not disclose, teach, or suggest a capacitive storage node comprising a binary scaled capacitor network, as recited in claims

1 and 15. Nor does Merrill et al. teach or suggest these limitations. Thus, Merrill et al. does not remedy the deficiencies of Sauer.

In view of the above, Applicants believe the pending application is in condition for allowance.

Dated: November 27, 2007

Respectfully submitted,

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